TGS8430

Discrete input and output interface circuit

Data sheet

Description

TGS8430 is a discrete input and output interface circuit that provides 8 channels of discrete to TTL level conversion and 4 channels of 200 mA high-side current output functions. Support SUPPLY/OPEN, GND/OPEN input model. The discrete comparison threshold can be selected as an internal threshold or an external threshold by configuring the $\overline{\text{THS\_SEL}}$ pin.

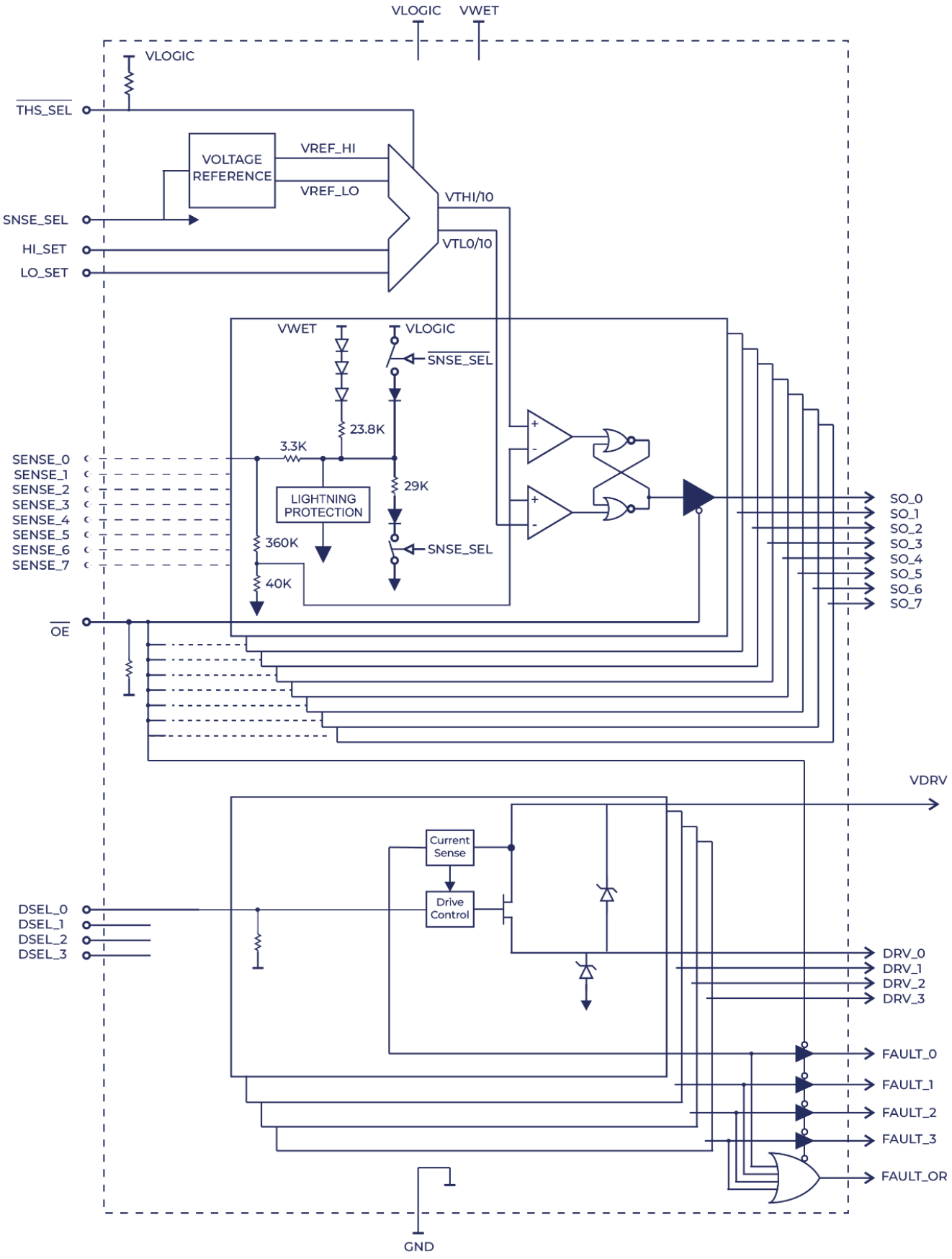
The 4 high-side outputs drive each output 200 mA current.

Logic pins are 5 V or 3.3 V compatible. The discrete input port lightning indirect effect protection level is RTCA-DO-160G Section 22 AZ, BZ and ZZ; The package is plastic QFN-40 and LQFP-44. The device quality level is N level (temperature cycle 500 times, HAST test 96h) standard specified in GJB 7400-2011.

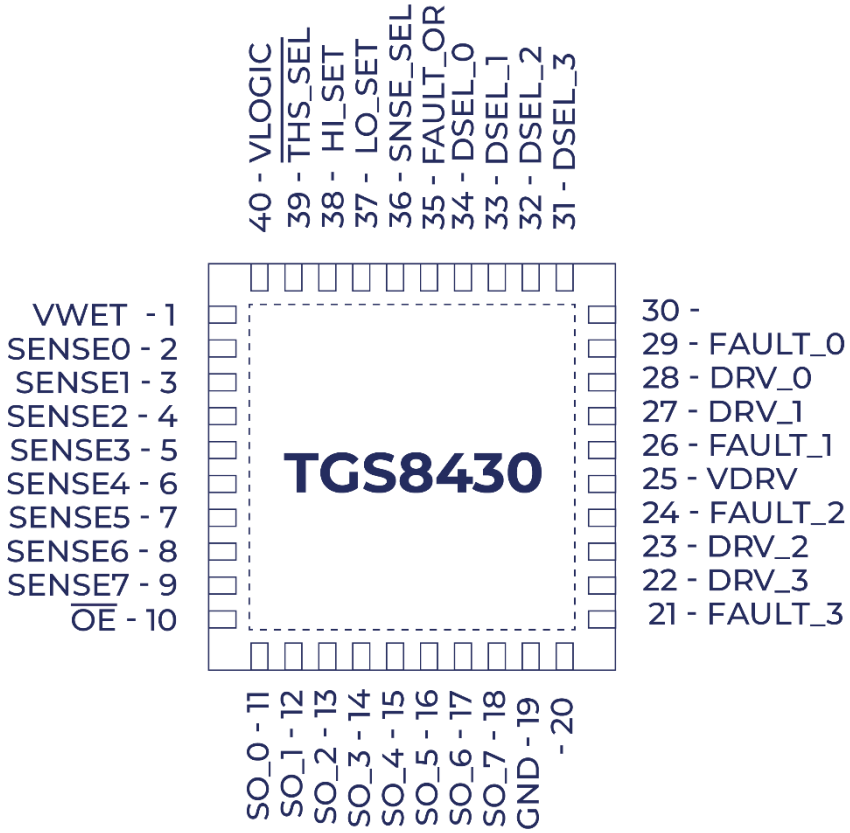
Characteristic

- Support SUPPLY/OPEN, GND/OPEN type discrete input;
- Provide 8 channels of discrete input;
- 4-channel high-side 200 mA current drive;
- Built-in/external discrete comparison threshold selection;
- The flip threshold and hysteresis voltage can be set;
- Overcurrent protection monitoring signal logic output;
- Discrete port lightning indirect effect protection function;
- Working temperature: -55℃ ~ 125℃;
- The power supply range is 3 V ~ 5.5 V;
- The package is plastic QFN-40, LQFP-44.

Block Diagram



Pin description



40 PIN PLASTIC 6MM X 6MM
CHIP-SCALE PACKAGE

Port number	Type	Signal name	Describe
1	Power supply	VWET	Optional input. In GND/OPEN operating mode, it provides dry/wet current to the relay. (The pin has a built-in 50 kΩ pull-down resistor)
2	Enter	SENSE0	Discrete input
3	Enter	SENSE1	
4	Enter	SENSE2	
5	Enter	SENSE3	
6	Enter	SENSE4	
7	Enter	SENSE5	
8	Enter	SENSE6	
9	Enter	SENSE7	

10	Enter	$\overline{OE}$	If it is logic "1", then SO_n outputs high impedance; if it is logic "0", then SO_n output data. (The pin has a built-in 30kΩ pull-down resistor)
11	Output	SO_0	Parallel data output
12	Output	SO_1	
13	Output	SO_2	
14	Output	SO_3	
15	Output	SO_4	
16	Output	SO_5	
17	Output	SO_6	
18	Output	SO_7	
19	Land	GND	Land
20	-	-	-
21	Output	FAULT_3	Driver_3 overcurrent fault indication
22	Output	DRV_3	Channel «3» 200 mA high side driver
23	Output	DRV_2	Channel «2» 200 mA high side driver
24	Output	FAULT_2	Driver_2 overcurrent fault indication
25	Power supply	VDRV	Driver power supply
26	Output	FAULT_1	Driver_1 overcurrent fault indication
27	Output	DRV_1	Channel «1» 200mA high side driver
28	Output	DRV_0	Channel «0» 200mA high side driver
29	Output	FAULT_0	Driver_0 overcurrent fault indication
30	-	-	-
31	Enter	DSEL_3	200 mA high-side drive input signal
32	Enter	DSEL_2	
33	Enter	DSEL_1	
34	Enter	DSEL_0	
35	Output	FAULT_OR	Any of the 4-channel Driver’s current fault display
36	Enter	SNSE_SEL	Ground/On or Power/On selection

37	Enter	LO_SET	If $\overline{\text{THS\_SEL}}$ is logic “1”, this pin sets the discrete comparison lower threshold
38	Enter	HI_SET	If $\overline{\text{THS\_SEL}}$ is logic “1”, this pin sets the discrete comparison high threshold
39	Enter	$\overline{\text{THS\_SEL}}$	Internal/external comparison threshold selection. A logic '1' selects the external threshold; a logic '0' selects the internal threshold.
40	Power supply	VLOGIC	Digital logic power supply (3.0 V -5.5 V)

Basic menu

SENSE_n	SNSE_SEL	$\overline{\text{THS\_SEL}}$	SO_n
Open circuit or $V_{SENSE\_n} > V_{THI}$	L (GND/OPEN mode)	L	L
$V_{SENSE\_n} < V_{TLO}$	L (GND/OPEN mode)	L	H
X	L (GND/OPEN mode)	H	Z
Open circuit or $V_{SENSE\_n} < V_{TLO}$	H (SUPPLY/OPEN mode)	L	H
$V_{SENSE\_n} > V_{THI}$	H (SUPPLY/OPEN mode)	L	L
X	H (SUPPLY/OPEN mode)	H	Z
Note: H = VLOGIC, L = GND, Z = Hi-Z, X is any value. For the values of VTHI and VTLO, please refer to the threshold selection table.			

Internal mode selection threshold ($\overline{\text{THS\_SEL}}$ = GND)

VLOGIC	VWET	SNSE_SEL	Model	High threshold window	Low threshold window
3.0 V	8 V	L	GND/OPEN	3.0 V	1.0 V
3.6 V	8 V	L	GND/OPEN	3.25 V	1.0 V
3.3 V	28 V	L	GND/OPEN	3.0 V	1.0 V
3.0 V ~ 3.6 V	OPEN	H	SUPPLY/OPEN	18.0 V	9.0 V
4.5 V	OPEN	L	GND/OPEN	3.5 V	1.0 V
5.5 V	OPEN	L	GND/OPEN	4.0 V	1.0 V
5.0 V	28 V	L	GND/OPEN	4.0 V	1.0 V
4.5 V ~ 5.5 V	OPEN	H	SUPPLY/OPEN	18.0 V	9.0 V

External mode selection threshold ($\overline{\text{THS\_SEL}}$ = VLOGIC)

VLOGIC	VWET	SNSE_SEL	Model	HI_SET set maximum value (V_{THI})	LO_SET Set minimum value (V_{TLO})	High threshold window	Low threshold window
3.0 V ~ 3.6 V	8 V	L	GND/OPEN	0.4 V (4 V)	0.3 V (3 V)	V_{THI}×1.25	V_{TLO}×0.75
3.0 V ~ 3.6 V	28 V	L	GND/OPEN	2.0 V (20 V)	0.3 V (3 V)		
3.0 V ~ 3.6 V	OPEN	H	SUPPLY/OPEN	2.2 V (22 V)	0.3 V (3 V)		
4.5 V ~ 5.5 V	7 V	L	GND/OPEN	0.4 V (4 V)	0.3 V (3 V)		
4.5 V ~ 5.5 V	28 V	L	GND/OPEN	2.0 V (20 V)	0.3 V (3 V)		
4.5 V ~ 5.5 V	OPEN	H	SUPPLY/OPEN	2.2 V (22 V)	0.3 V (3 V)		
Note: V_{THI} = HI_SET×10, V_{TLO} = LO_SET×10.							

Extreme working conditions

Parameter		Minimum value	Maximum value	Unit
Supply voltage (VLOGIC)		-0.3	7	V
VDRV			50	V
VWET		-0.3	50	V
The maximum current that the Driver port can withstand			300	mA
LOGIC input voltage range		-0.3	VLOGIC+0.3	V
Discrete input voltage range		-80	80	V
Heat dissipation power (T_A = +70℃)	QFN		1.7	W
Welding temperature			260	℃
Junction temperature			175	℃
Storage temperature		-150	65	℃

Recommended working conditions

Parameter		Minimum value	Maximum value	Unit
Supply voltage	VLOGIC	3	5.5	V
	VDRV	7	36	V
	VWET	8	36	V
Operating temperature range		-55	125	℃

DC characteristics

Name	Parameter	Test conditions (If no special instructions are given, the test temperature for all test items is T_A= -55˚C to 125˚C)	Smallest	Typical	Maximum	Unit
GND/OPEN mode						
Resistance	R_{IN}	Impedance RIN from input port to VLOGIC		3.3		KΩ
	R_W	Impedance RW from input port to VWET		23.8		KΩ
Wet current	I_{WET}	VWET = open			1	mA
$\overline{\text{THS\_SEL}}$ = GND						
Ground input voltage	V_{GS}	When the logic output is high, the input port is connected to ground voltage			1	V
On input voltage	V_{OS}	VDD = 5.5 V	4			V
		VDD = 3 V	3			V
Input current	I_{IN28}	VIN = 0 V, VDD = 3.0 V		-0.65		mA
		VIN = 0 V, VDD = 5.5 V		-1.65		mA
Hysteresis voltage	VHY	Hysteresis voltage	0.15			V
$\overline{\text{THS\_SEL}}$ = Open or VLOGIC						
HI_SET high threshold range	V_{THI}	The high comparison threshold is HI_SET*10	0.4		2	V
LO_SET low threshold range	V_{TLO}	The low comparison threshold is LO_SET*10	0.3		1.9	V
Minimum threshold window	V_{THW}	HI_SET > LO_SET	0.1			V
Threshold accuracy	V_{THA}	See the threshold selection table for relevant input voltages.	V_{TLO}× 0.75		V_{THI} × 1.25	V
SUPPLY/OPEN mode						
Resistance	R_{IN}	Input port to ground resistance		30		KΩ
$\overline{\text{THS\_SEL}}$ = GND						

On input voltage	V_{OS}	When the logic output is high, the input port is connected to ground voltage			9	V
V+ state input voltage	V_{V+}	When the logic output is low, the input port is connected to ground voltage	18			V
Input current	I_{IN28}	V_{IN} = 28 V		0.95		mA
Hysteresis voltage	V_{HY}	Hysteresis voltage	1.5			V
$\overline{\text{THS\_SEL}}$ = Open or VLOGIC						
HI_SET high threshold range	V_{THI}	The high comparison threshold is HI_SET*10	0.4		2.2	V
LO_SET low threshold range	V_{TLO}	The low comparison threshold is LO_SET*10	0.3		2.1	V
Minimum threshold window	V_{THW}	HI_SET>LO_SET	0.1			V
Threshold accuracy	V_{THA}	See the threshold selection table for relevant input voltages.	V_{TLO}× 0.75		V_{THI} × 1.25	V
Logic input						
Input voltage	V_{IH}	Input high voltage HI	0.8			VLOGIC
	V_{IL}	Input low voltage LO			0.2	VLOGIC
$\overline{\text{OE}}$, DSEL_n port input current	I_{SINK}	V_{IN} = VLOGIC, 30 KΩ pull-down resistor		125		uA
	I_{SOURCE}	V_{IN} = GND			0.1	uA
$\overline{\text{THS\_SEL}}$ port input current	I_{SINK}	V_{IN} = VLOGIC			0.1	uA
	I_{SOURCE}	V_{IN} = GND, 30 KΩ pull-up resistor		125		uA
SNSE_SEL port input current	I_{SINK}	VIN = VLOGIC			0.1	uA
	I_{SOURCE}	V_{IN} = GND			0.1	uA
Logic output						
Output voltage	V_{OH}	I_{oH} = -100 uA	90%			VLOGIC

	V_{OL}	I_{oH} = 100 uA			10%	VLOGIC
Output current	I_{OL}	V_{out} = 0.4 V	1.6			mA
	I_{OH}	V_{out} = V_{LOGIC}-0.4 V			-1	mA
Three-state leakage current	I_{TSL}	Vlogic > Vout > GND	-1		1	uA
Output capacitor	Co	Output capacitor		15		pF
Analog input						
HI_SEL/LO_SET port leak leakage current	I_L	VLOGIC > V_{input} > GND	-0.1		1	uA
Current						
VLOGIC port current	I_{DD1}	All ports left open			10	mA
VWET port current	I_{VWET}	All input pins are 0 V, VWET = 28 V			20	mA
High side driver						
On-resistance	R_{ON}	V_{DRV} = 28 V, I_{SOURCE} = 200 mA		4.5	8	Ω
Overcurrent shutdown voltage	V_{DCMAX}	Maximum V_{DS} value before current is limited	1.5			V
Overcurrent protection delay time	T_{OC}	Before the driver's maximum current begins to decrease takes time	5	11		us

AC characteristics

Name	Parameter	Test conditions (If no special instructions are given, the test temperature for all test items is T_A= -55˚C to 125˚C)	Smallest	Typical	Maximum	Unit
SUPPLY/OPEN mode						
Delay when output is high	t_{H1}	See Figure 1, $\overline{THS\_SEL}$ = GND, 25℃		1		us
Delay when output is low	t_{L1}	See Figure 1, $\overline{THS\_SEL}$ = GND, 25℃		1		us

GND/OPEN mode						
Delay when output is high	t_{H2}	See Figure 2, $\overline{THS\_SEL}$ = GND, 25℃		1		us
Delay when output is low	t_{L2}	See Figure 2, $\overline{THS\_SEL}$ = GND, 25℃		1		us
Tri-state delay						
Delay during tri-state turn-on	t_{TSON}	See Figure 3, $\overline{THS\_SEL}$ = GND, 25℃			40	ns
Tri-state shutdown delay	t_{TSOFF}	See Figure 3, THS_SEL = GND, 25℃			40	ns
High side driver						
Drive circuit turn-on delay	t_{SON}	See Figure 4, VLOGIC = 3.3 V, 25℃	400			ns
Driver circuit turn-off delay	t_{SOFF}	See Figure 4, VLOGIC = 3.3 V, 25℃			900	ns
Overcurrent protection circuit turn-on delay	t_{FON}	See Figure 5, VLOGIC = 3.3 V, 25℃			15	us
Overcurrent protection circuit shutdown delay	t_{FOFF}	See Figure 5, VLOGIC = 3.3 V, 25℃			15	us

Delay waveform

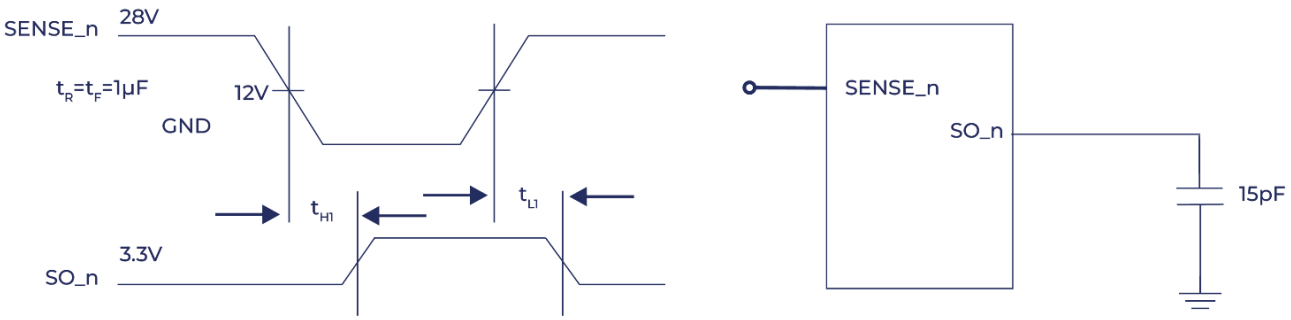


Figure 1. 28V/OPEN output delay

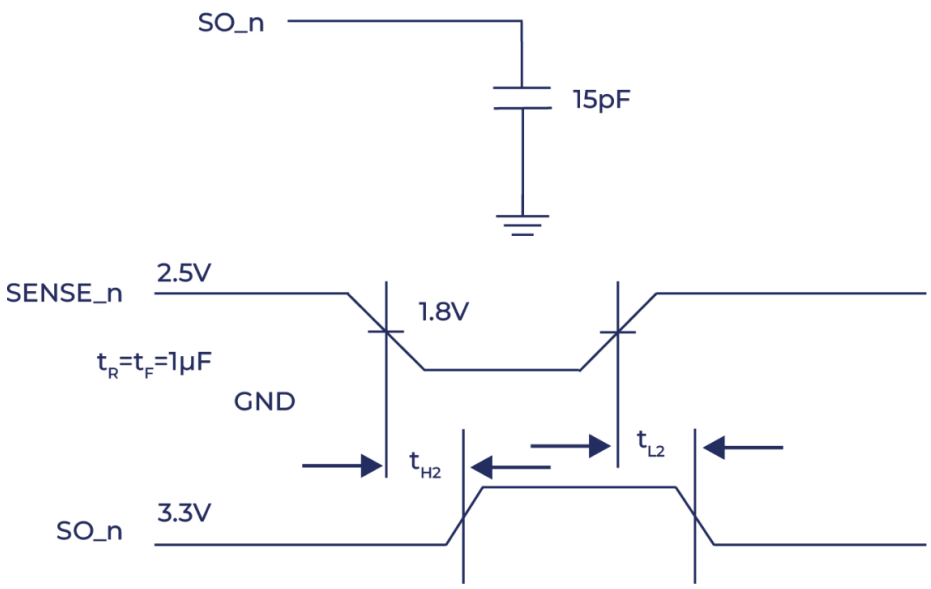


Figure 2. GND/OPEN output delay

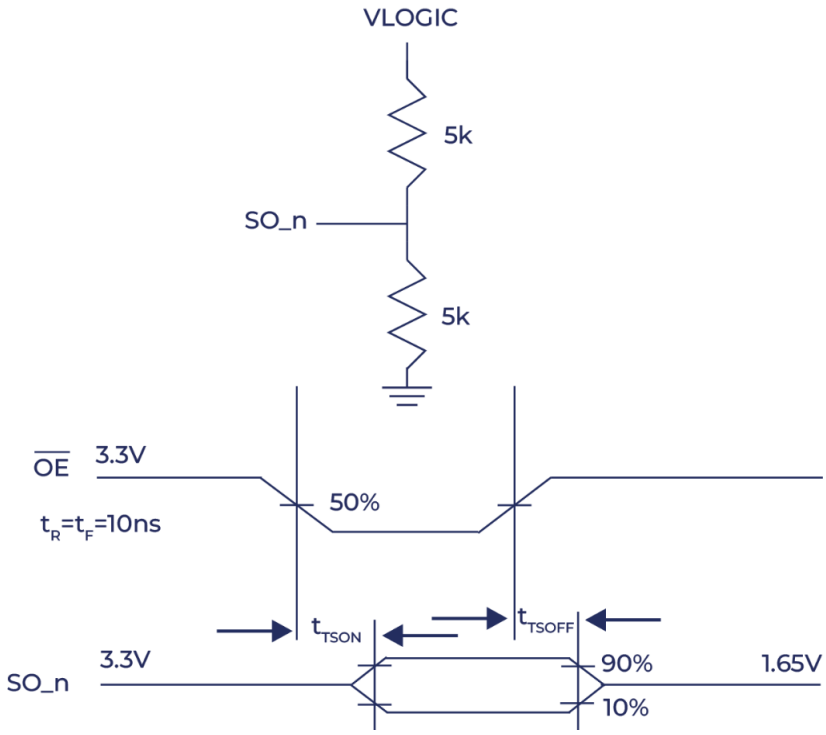


Figure 3. $\overline{OE}$ enable terminal output delay

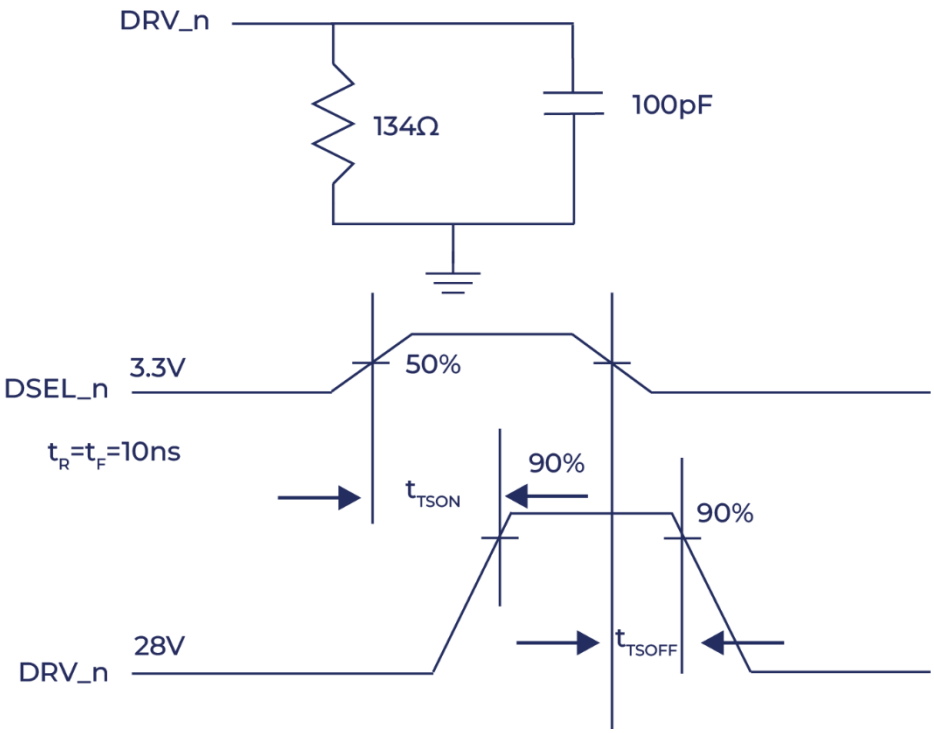


Figure 4. High-side driver output delay

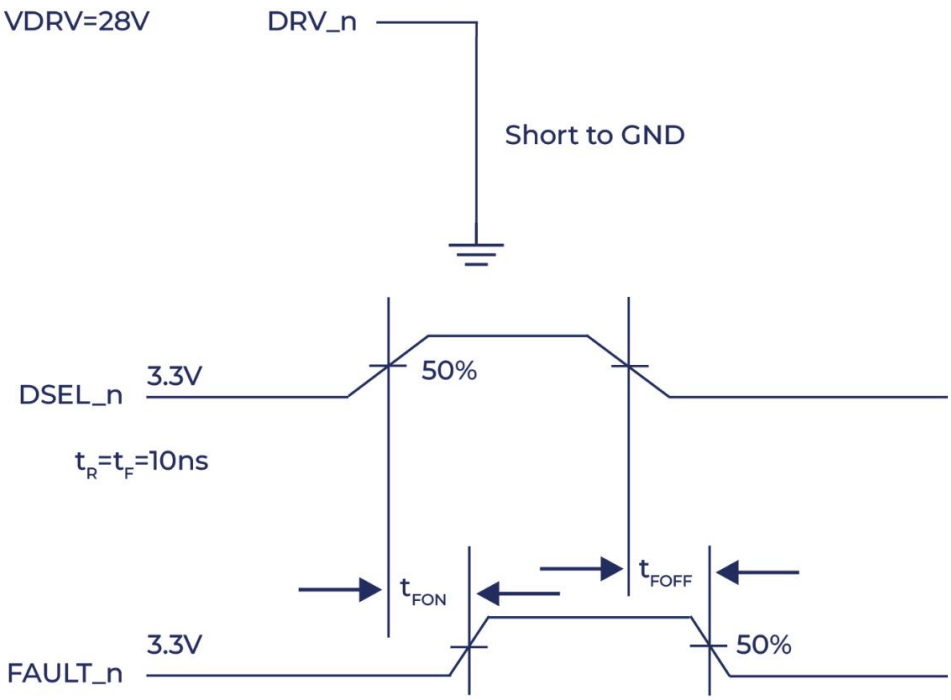
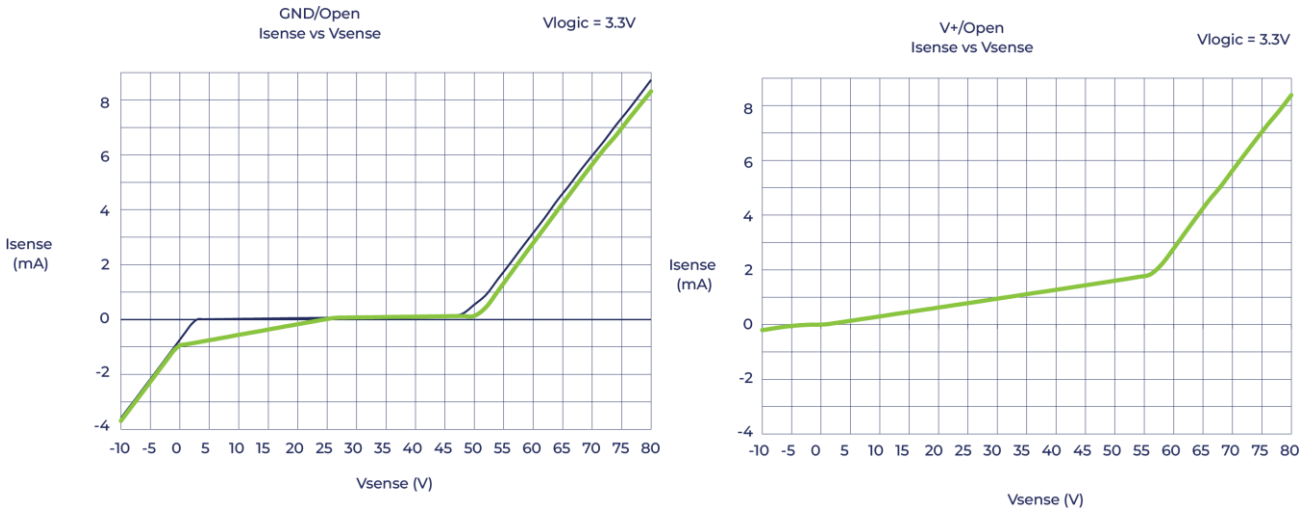


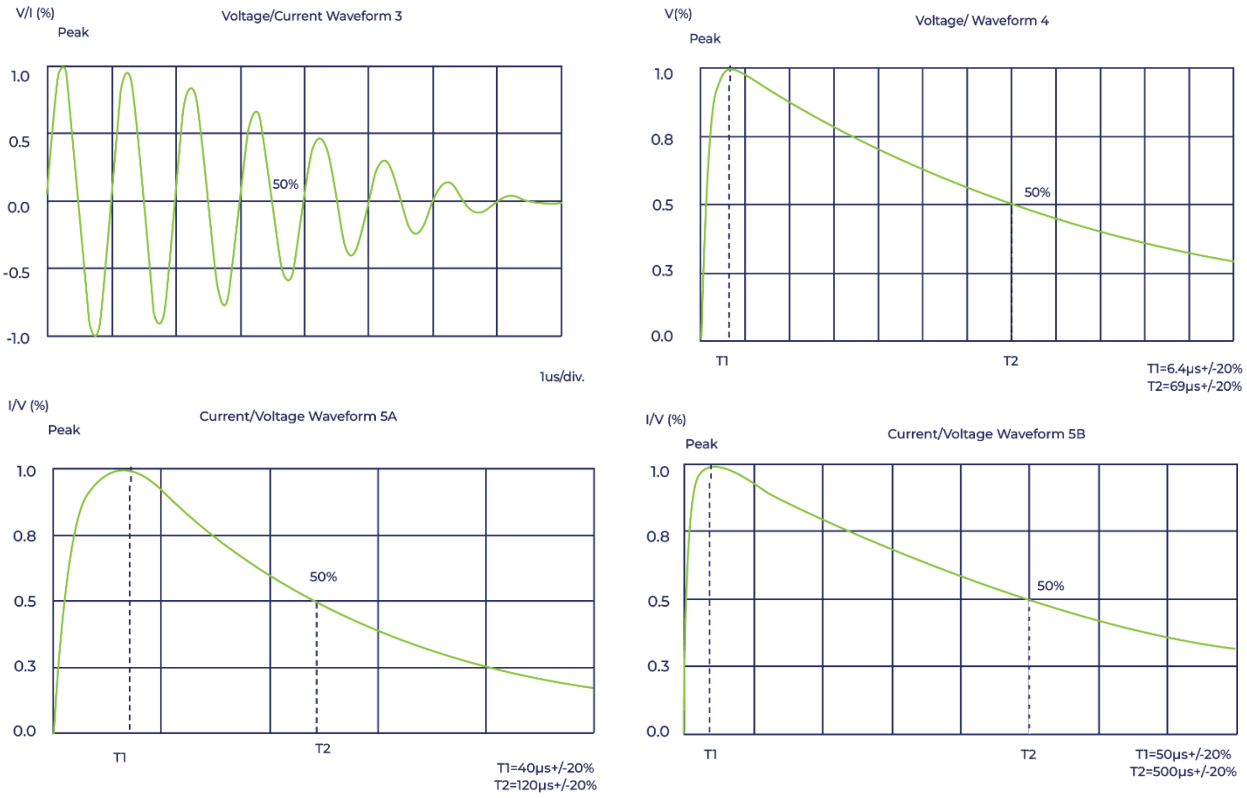
Figure 5. Detection delay when high-side driver is short-circuited

Wet current waveform



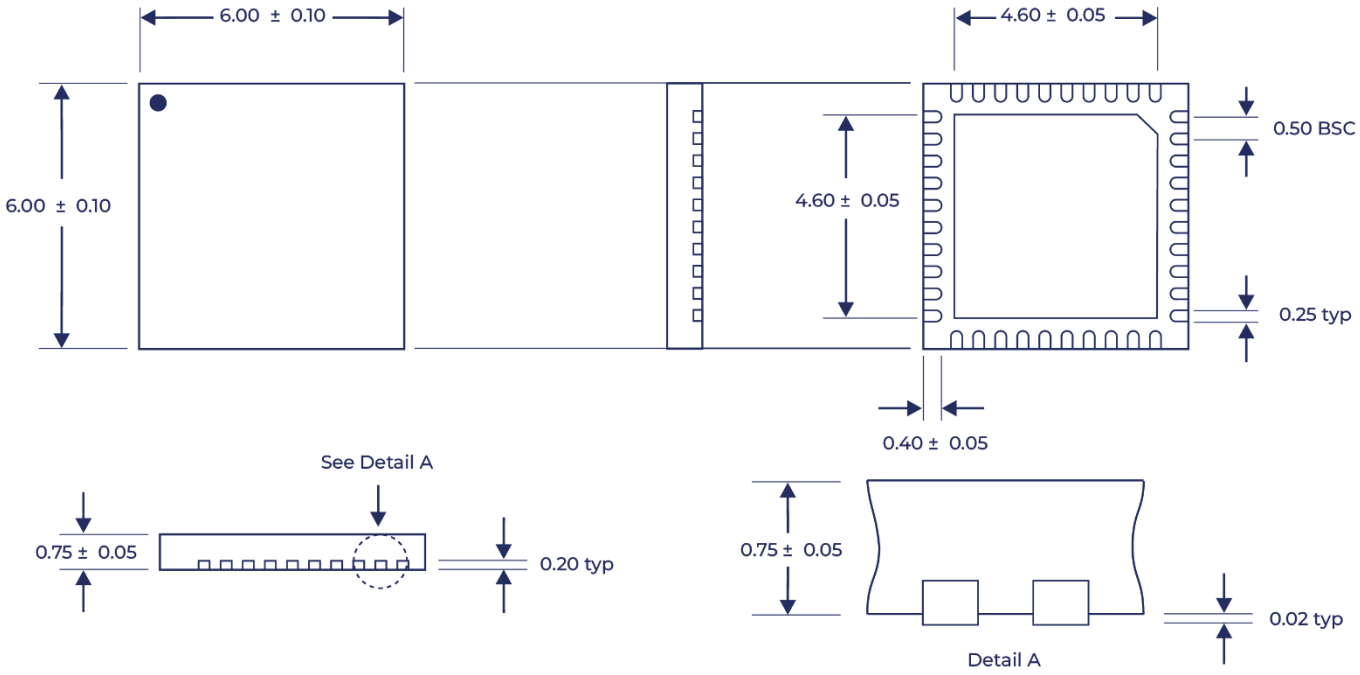
Lightning protection

Grade	Waveform			
	3/3	4/1	5A/5A	5B/5B
	Voc(V)/Isc(A)	Voc(V)/Isc(A)	Voc(V)/Isc(A)	Voc(V)/Isc(A)
2	250/10	125/25	125/125	125/125
Z	500/20	300/60	300/300	300/300
3	600/24	300/60	300/300	300/300

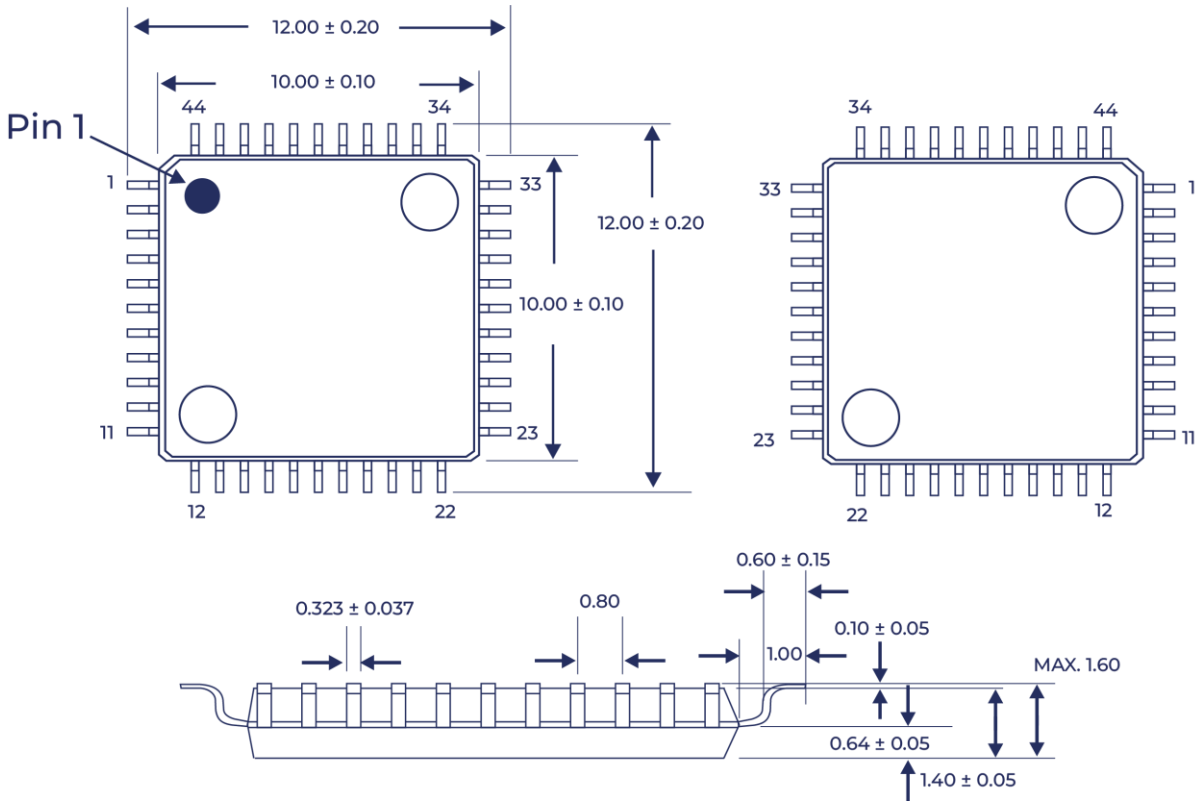


Overall dimensions parameters

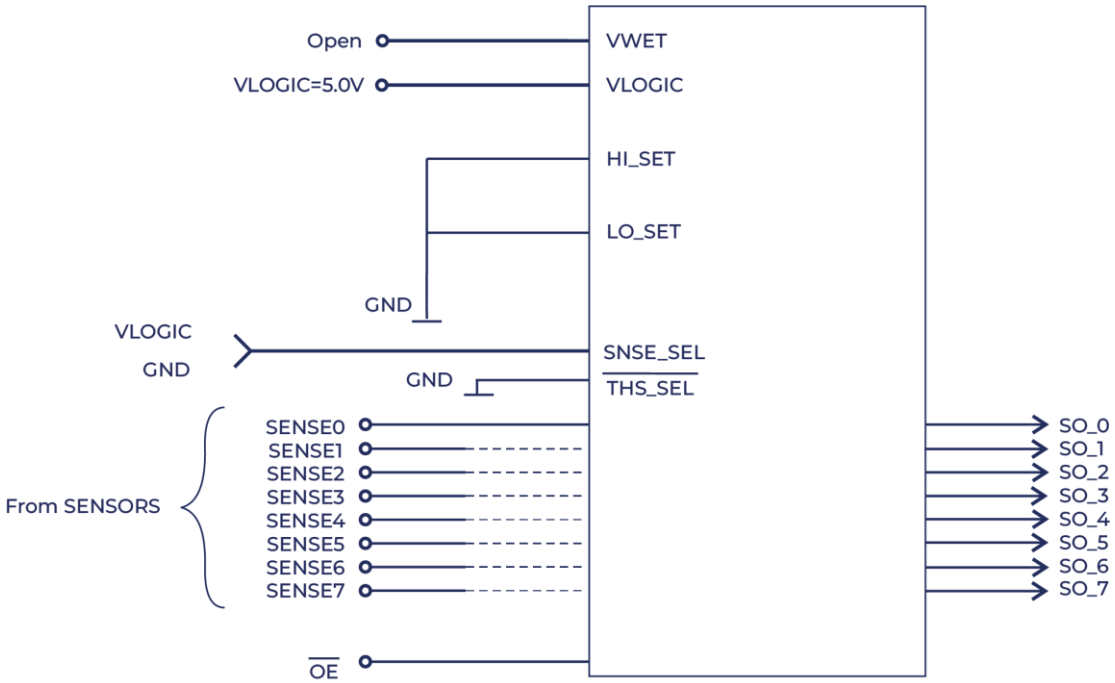
QFN-40



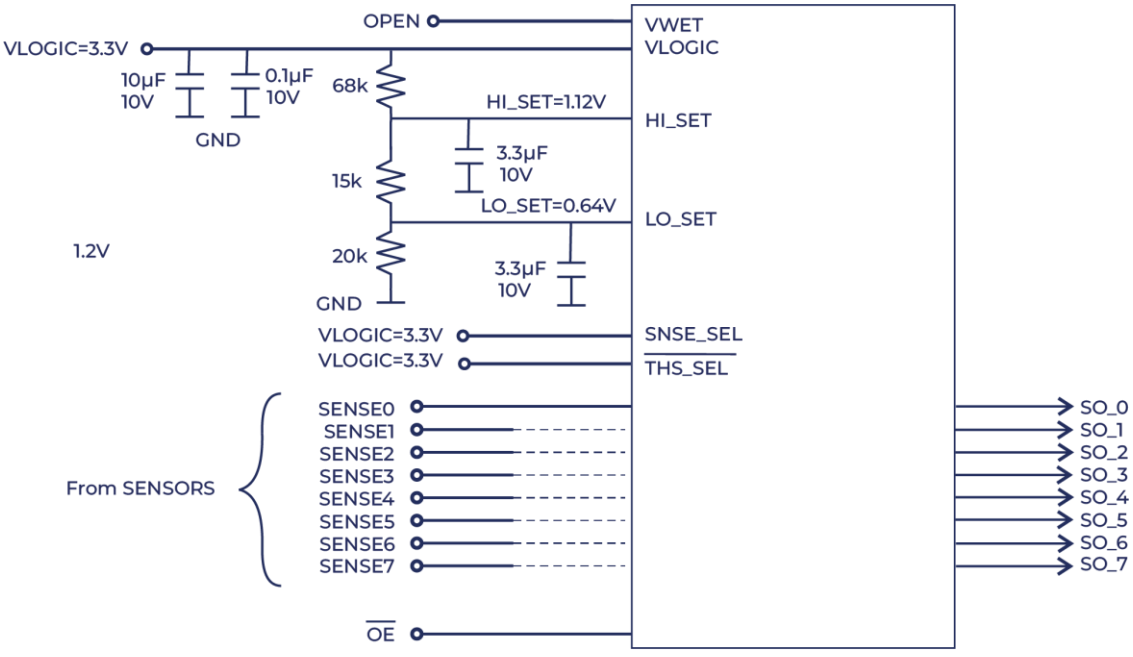
LQFP-44



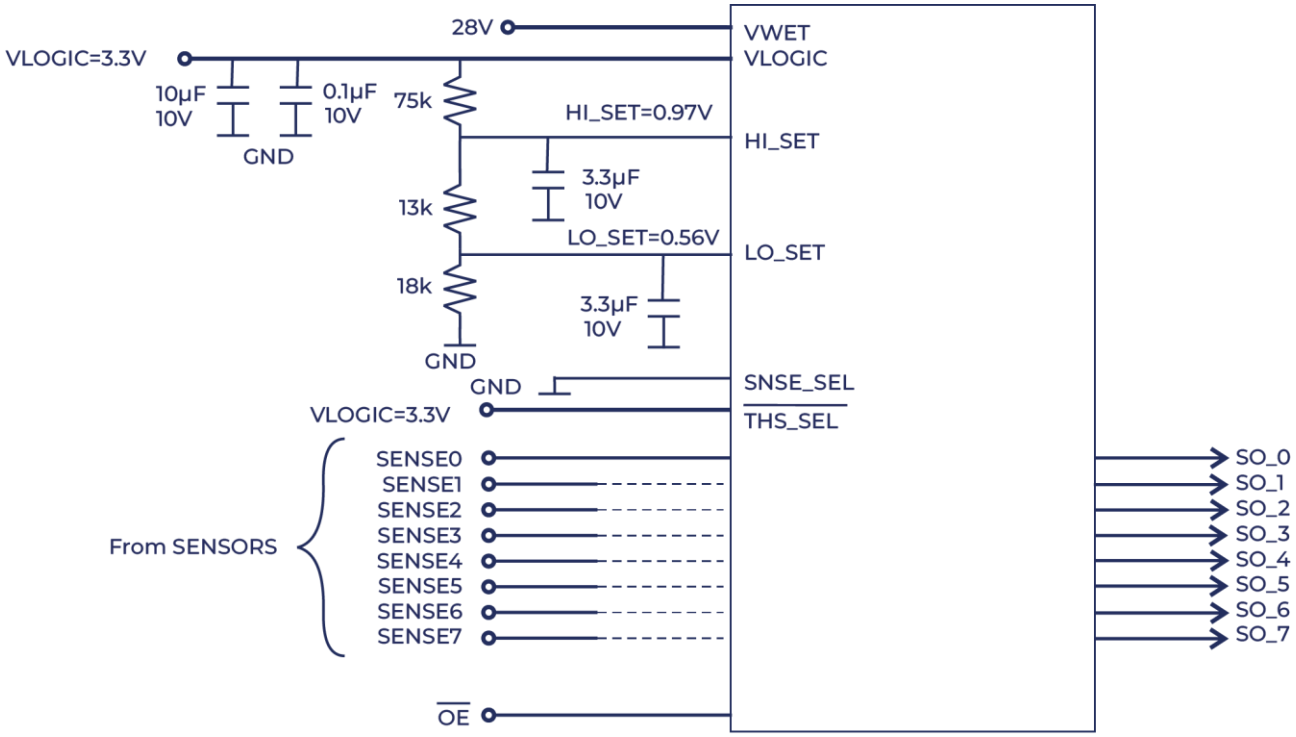
Application examples



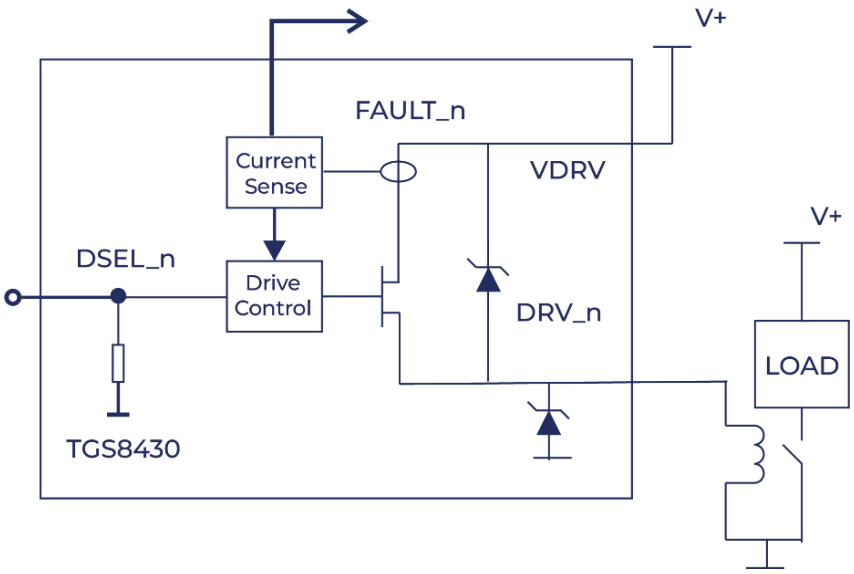
Configuring the graph using internal thresholds



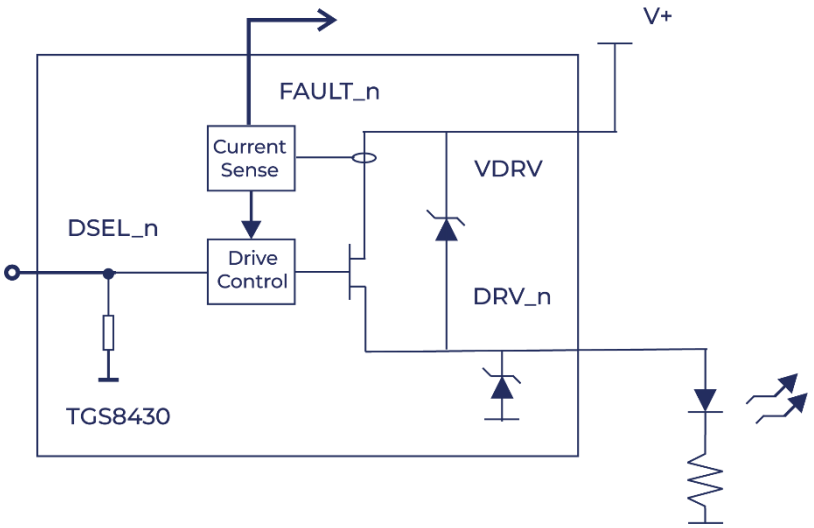
28V/OPEN ABD0100H threshold configuration diagram



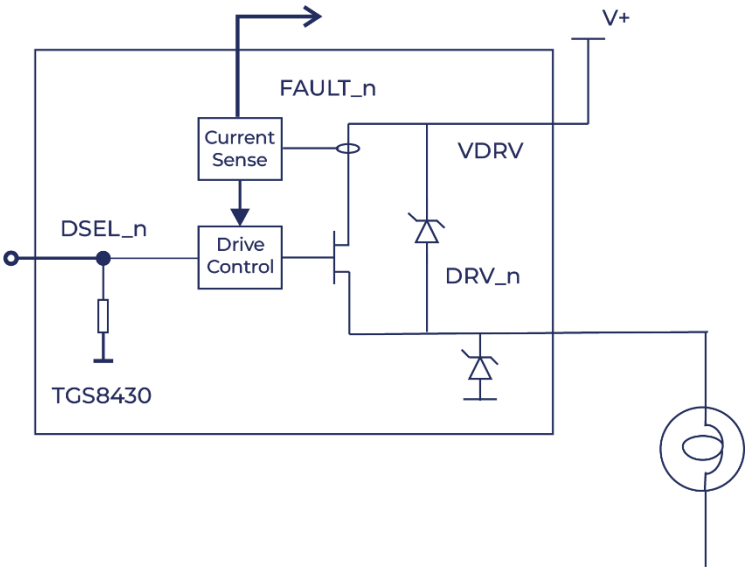
GND/OPEN ABD0100H threshold, 1mA wet current configuration diagram



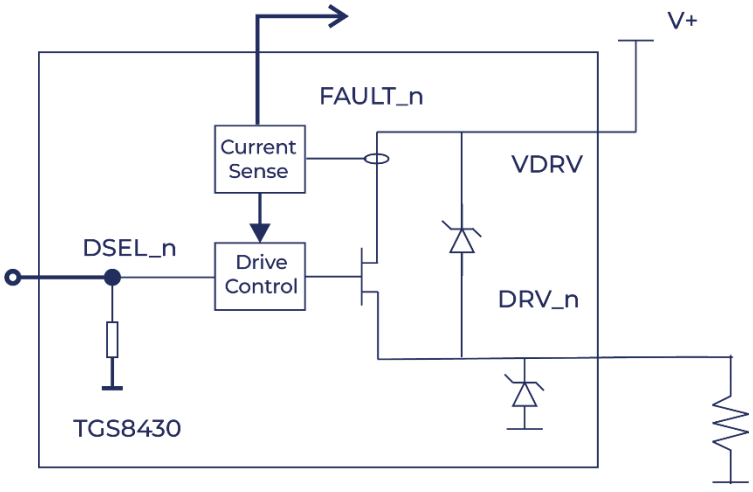
High side driver relay



High side driver LED



High side driving light



High-side driving resistive loads

Ordering information

Model	Package
TGS8430-PC	QFN40
TGS8430-LQ	LQFP44